Breakdown-resistant thin film capacitor with interdigitated structure.

BACKGROUND OF THE INVENTION

The invention relates to a thin film capacitor which comprises a carrier substrate, at least two interdigitated electrodes, and at least one dielectric.

Dielectric materials with high dielectric constant values ($\varepsilon_r > 50$) are used for achieving high capacitance values in capacitors of small dimensions. Dielectrics with $\varepsilon_r > 50$ at dielectric thicknesses of 50 nm to 2 µm are made by means of thin film processes in the manufacture of of thin film capacitors. An inexpensive method which is used for depositing thin layers with $\varepsilon_r > 50$ is a wet chemical thin film method such as, for example, the sol-gel method. The lower electrode in a thin film capacitor is made of a non-noble metal such as, for example, aluminum or copper, or a noble metal, for example silver, a silver alloy, or platinum. For the upper electrode, noble metals such as, for example, platinum, silver, silver alloys, or NiCr/gold are used, as for the lower electrode, or alternatively non-noble metals such as, for example, aluminum, nickel, or copper. These are applied by means of thin film processes such as, for example, sputtering or chemical deposition from the gas phase. The electrodes are structured by means of lithographical processes in combination with wet or dry etching steps. Suitable carrier substrate materials are Si wafers, glass or ceramic materials. A protective layer is used for protecting the capacitor construction, for example an organic layer and/or an inorganic layer provided in a printing process or a thin film process. The capacitors are further provided with current supply contacts, either individually or in rows.

This state of the art technology is quite capable of producing inexpensive thin film capacitors which comply with standard specifications. The layer thicknesses of approximately one micrometer, however, do not suffice if higher operating voltages U_{rated} (50 V, 100 V and higher) are to be accommodated in conjunction with increased life requirements for low capacitance values of a few picofarad in high-frequency applications.

A higher breakdown resistance is found in so-called interdigitated capacitors whose electrodes have a finger-like arrangement. The finger shapes of these interdigitated electrodes and their interlocking arrangement together with the superimposed dielectric form the actual capacitor. The capacitance value of such an arrangement is a function of the finger interspacing, the length of the overlaps, the thickness of the dielectric, the dielectric constant values of the substrate and of the dielectric, and the thickness of the electrodes. The finger

interspacing in fact determines the breakdown resistance and the resulting admissible operating voltage of the capacitor type.

A capacitor arrangement with interdigitated electrodes is known from publication no. 07283076 A from "Patent Abstracts of Japan", wherein several interdigitated electrode layers are present one above the other so as to enhance the capacitance value still further. The interdigitated electrodes of a capacitor unit all lie in one plane, and a dielectric is present between every two adjoining electrode levels. A disadvantage of the arrangement of the electrodes in one plane is that the full thickness of the dielectric is not utilized for contributing to the capacitance of the capacitor.

SUMMARY OF THE INVENTION

The invention has for its object to develop an improved thin film capacitor with interdigitated electrodes and a high breakdown resistance.

This object is achieved in a thin film capacitor comprising a carrier substrate, at least two interdigitated electrodes, and at least one dielectric, which is characterized in that at least one interdigitated electrode is arranged below the dielectric and at least one interdigitated electrode is arranged above the dielectric.

The layers of the dielectric contribute to the capacitance behavior of the capacitor when the interdigitated electrodes are positioned above and below the dielectric.

A preferred embodiment provides that the interdigitated electrode above the dielectric is positioned staggered with respect to the interdigitated electrode below the dielectric.

The staggered arrangement achieves that the dielectric is permeated more evenly by the electric field, and accordingly higher capacitance values can be attained, all other parameters remaining the same.

A further preferred embodiment is characterized in that the dielectric comprises a plurality of layers.

It is possible through the use of multiple layers, for example double, triple, or quadruple layers, to compensate for the unfavorable temperature behavior of some dielectric materials and to improve the temperature dependence of the capacitance value of the thin film capacitor.

In a preferred embodiment, the dielectric comprises a ferroelectric ceramic material.

Ferroelectric ceramic materials have a high relative dielectric constant ε_r annnd allow for high capacitance values in small dimensions.

It is furthermore preferred that a barrier layer is provided on the carrier substrate.

Reactions with the dielectric or short-circuits can be avoided by means of a barrier layer in the case of substrates having a rough surface, for example Al_2O_3.

~~The invention will be explained in more detail below with reference to a Figure and two embodiments, with:~~

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

Fig. 1 ~~being~~ is a diagram of the construction of a thin film capacitor with two interdigitated electrodes, and

Fig. 2 ~~being~~ is a diagram of the construction of a thin film capacitor with three interdigitated electrodes.

DETAILED DESCRIPTION OF THE INVENTION

In Fig. 1, a thin film capacitor comprises a carrier substrate 1 which is made, for example, from a ceramic material, a glass-ceramic material, a glass material, or silicon. A barrier layer, for example made from SiO_2, TiO_2, Al_2O_3 or ZrO_2, is provided on the carrier substrate 1. On this barrier layer 2 there is a first interdigitated electrode 4 which comprises, for example, Al,

Al doped with Cu,

Cu,

W,

Pt,

Ni,

Pd,

Pd/Ag,

TiW/Al,

Ti/Pt,

Ti/Ag,

Ti/Ag/TiIr,

Ti/Ag_xPt_{1-x} $(0 \leq x \leq 1)$

$Ti/Ag/Pt_xAl_{1-x}$ $(0 \leq x \leq 1)$,

$Ti/Ag_xPt_{1-x}/Ir$ $(0 \leq x \leq 1)$,

$Ti/Ag/(Ir/IrO_x)$ $(0 \leq x \leq 2)$,

$Ti/Ag/Ru_xPt_{1-x}$ $(0 \leq x \leq 1)$,

$Ti/Pt_xAl_{1-x}/Ag/Pt_yAl_{1-y}$ $(0 \leq x \leq 1,\ 0 \leq y \leq 1)$,

$Ti/Ag/Pt_y(RhO_x)_{1-y}$ $(0 \leq x \leq 2,\ 0 \leq y \leq 1)$,

$Ti/Ag/Pt_xRh_{1-x}$ ($0 \leq x \leq 1$),

$Ti/Ag_xPt_{1-x}/(Ir/IrO_y)$ ($0 \leq x \leq 1$, $0 \leq y \leq 2$),

$Ti/Ag_xPt_{1-x}/Pt_yAl_{1-y}$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$),

Ti/Ag/Ti,

Ti/Ni/ITO or

$NiCrAl/Ni$, $Ni_xCr_yAl_z/Ni$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$).

A dielectric 3 having a high relative dielectric constant $\varepsilon_r > 20$ is provided on the lower interdigitated electrode 4. The dielectric 3 may comprise, for example, $Pb(Zr_xTi_{1-x})O_3$ ($0 \leq x \leq 1$) with and without excess lead,

$(Pb,Ba)(Mg_{1/3}Nb_{2/3})_x(Zn_{1/3}Nb_{2/3})_yTi_zO_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$),

$Ba_{1-x}Sr_xTiO_3$ ($0 \leq x \leq 1$),

$Pb_{1-1.5y}La_y(Zr_xTi_{1-x})O_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 0.2$),

$SrTi_{1-x}Zr_xO_3$ ($0 \leq x \leq 1$),

$(Zr,Sn)TiO_4$,

Ta_2O_5 with Al_2O_3 dopants,

$Pb_{1-\alpha y}\ La_yTiO_3$ ($0 \leq y \leq 0.3$, $1.3 \leq x \leq 1.5$),

$(Pb,Ca)TiO_3$,

$BaTiO_3$ with and without dopants,

$Ba_2Ti_9O_{20}$,

$CaSm_2Ti_5O_{14}$,

$TiZr_{0.8}Sn_{0.2}O_4$,

$Ba_2Ti_{8.53}Zr_{0.50}Mn_{0.01}O_{20}$,

$SrZr_xTi_{1-x}O_3$ ($0 \leq x \leq 1$) with and without Mn dopants,

$BaZr_xTi_{1-x}O_3$ ($0 \leq x \leq 1$),

$Ba_{1-y}Sr_yZr_xTi_{1-x}O_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$),

$SrTiO_3$ doped with, for example, La, Nb, Fe or Mn,

$(BaTiO_3)_{0.18-0.27} + (Nd_2O_3)_{0.316-0.355} + (TiO_2)_{0.276-0.355} + (Bi_2O_3)_{0.025-0.081} + x\ ZnO$,

$CaZrO_3$,

$CaTiO_3 + CaTiSiO_5$,

$(Sr,Ca)(Ti,Zr)O_3$,

$(Sr,Ca,M)(Ti,Zr)O_3$ (M= Mg or Zn),

$(Sr,Ca,Cu,Mn,Pb)TiO_3 + Bi_2O_3$,

$BaO\text{-}TiO_2\text{-}Nd_2O_3\text{-}Nb_2O_5$,

$(Ba,Ca)TiO_3 + Nb_2O_5$, Co_2O_3, MnO_2,

TiO_2,

$BaO\text{-}PbO\text{-}Nd_2O_3\text{-}TiO_2$,

$Ba(Zn,Ta)O_3$,

$BaZrO_3$,

$Nd_2Ti_2O_7$,

$PbNb_x((Zr_{0.6}Sn_{0.4})_{1-y}Ti_y))_{1-x}O_3$ ($0 \leq x \leq 0.9$, $0 \leq y \leq 1$),

$Pb(Mg_{1/3}Nb_{2/3})O_3]_x\text{-}[PbTiO_3]_{1-x}$ ($0 \leq x \leq 1$),

$(Pb,Ba,Sr)(Mg_{1/3}Nb_{2/3})_xTi_y(Zn_{1/3}Nb_{2/3})_{1-x-y}O_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$), $x + y \leq 1$)

a) $Pb(Mg_{1/2}W_{1/2})O_3$

b) $Pb(Fe_{1/2}Nb_{1/2})O_3$

c) $Pb(Fe_{2/3}W_{1/3})O_3$

d) $Pb(Ni_{1/3}Nb_{2/3})O_3$

e) $Pb(Zn_{1/3}Nb_{2/3})O_3$

f) $Pb(Sc_{1/2}Ta_{1/2})O_3$

as well as combinations of the compounds a) to f) with $PbTiO_3$ and $Pb(Mg_{1/3}Nb_{2/3})O_3$.

An upper interdigitated electrode 5 is provided on the dielectric 3, which electrode comprises, for example, Al,

Al doped with Cu,

Cu,

W,

Pt,

Ni,

Pd,

Pd/Ag,

TiW/Al,

Ti/Pt,

Ti/Ag,

Ti/Ag/TiIr,

Ti/Ag_xPt_{1-x} ($0 \leq x \leq 1$),

$Ti/Ag/Pt_xAl_{1-x}$ ($0 \leq x \leq 1$),

$Ti/Ag_xPt_{1-x}/Ir$ ($0 \leq x \leq 1$),

$Ti/Ag/(Ir/IrO_x)$ ($0 \leq x \leq 2$),

$Ti/Ag/Ru_xPt_{1-x}$ ($0 \leq x \leq 1$),

$Ti/Pt_xAl_{1-x}/Ag/Pt_yAl_{1-y}$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$),

$Ti/Ag/Pt_y(RhO_x)_{1-y}$ ($0 \leq x \leq 2$, $0 \leq y \leq 1$),

$Ti/Ag/Pt_xRh_{1-x}$ ($0 \leq x \leq 1$),

$Ti/Ag_xPt_{1-x}/(Ir/IrO_y)$ ($0 \leq x \leq 1$, $0 \leq y \leq 2$),

$Ti/Ag_xPt_{1-x}/Pt_yAl_{1-y}$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$),

Ti/Ag/Ti,

Ti/Ni/ITO or

$Ni_xCr_yAl_z/Ni$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$)

Alternatively, the dielectric 3 may comprise multiple layers, for example double, triple, or quadruple layers.

In addition, a multiple layer structure may be implemented with three or more interdigitated electrodes in staggered arrangement.

Fig. 2 shows such a multiple layer arrangment with three staggered interdigitated electrodes 41, 42, and 51, and two dielectrics 31 and 32. In this embodiment of the thin film capacitor according to the invention, a first dielectric 31 is disposed over a first interdigitated electrode 41, over this a second interdigitated electrode 51 covered by a second dielectric layer 32, and a third interdigitated electrode 42. The first interdigitated electrode 41 and the third interdigitated electrode 42 are connected in parallel.

Embodiments of the invention which represent examples of how the invention may be realized in practice will now be explained in detail below.

Embodiment 1:

A carrier substrate 1 of glass is provided with a barrier layer 2 of TiO_2. A lower interdigitated electrode 4 of Ti/Pt is provided on this barrier layer 2. A dielectric 3 of $BaTiO_3$ is disposed over the lower interdigitated electrode 4. An upper interdigitated electrode 5 of Pt is provided on said dielectric 3.

Embodiment 2:

A carrier substrate 1 of glass is provided with a barrier layer 2 of TiO_2. . A lower interdigitated electrode 4 of Ti/Pt is provided on this barrier layer 2. A dielectric 3 of $Pb(Zr_{0.53}Ti_{0.47})O_3$ doped with lanthanum is disposed over the lower interdigitated electrode 4. An upper interdigitated electrode 5 of Pt is provided on said dielectric 3.

Standard monolayer capacitors are also manufactured in the same manufacturing process. The results of three tests are summarized in Table 1 below.

Table 1: Standard Monolayer Capacitor with 20 V/µm and 13 nF/mm^2

		Test 1	Test 2	Test 3	Average
Rel. Dielectric Constant ε_r		1120	1060	1070	1083
Dielectric	[µm]	0.754	0.784	0.702	0.747
Op. Voltage U_{rated}	[V]				15

Table 2: Parameters for the interdigitated electrodes

Number of Fingers:	12
Number of Gaps:	11
Length of Finger Overlap [µm]:	850
Total Overlap Length [µm]:	9350

Table 3 shows the average capacitance values C and the operating voltages U_{rated} for thin film capacitors with interdigitated electrodes (parameters in accordance with Table 2) and a lanthanum-doped PZT dielectric (layer thicknesses in accordance with Table 1).

Table 3: Average Capacitance Values C of Thin Film Capacitors with Interdigitated Electrodes and Lanthanum-Doped PZT Dielectric Layers.

Finger Interspacing [µm]	Capacitance C [pF]	Op. Voltage U_{rated} [V]
10	6.3	200
5	10.8	100
3	17.5	60